REMARKS/ARGUMENTS

1. Objection of claims 1 and 9:

Response:

Claims 1 and 9 have been amended to overcome this objection. Specifically, the limitation "each layout in the connection layer corresponding to each sub-circuit cell creates a connection between the sub-circuit blocks **within** each corresponding sub-circuit cell by selectively connecting the sub-circuit blocks within each corresponding sub-circuit cell" has been added to claims 1 and 9. This limitation finds support in paragraphs [0022]-[0024], and in Fig. 3 for instance, and no new matter is introduced. Claims 1 and 9 are now no longer unclear, and withdrawal of claims 1 and 9 is politely requested.

2. Rejection of claims 1-3, 5, 7-10, 12, 14, 15 under 35 U.S.C. 102 (e) as being anticipated by Schadt et al. (US 6,870,395):

Response:

Claims 1 and 9:

Claims 1 and 9 have been amended to overcome this rejection. Specifically, the limitation "each layout in the connection layer corresponding to each sub-circuit cell creates a connection selectively connected to between the sub-circuit blocks **within** each corresponding sub-circuit cell by selectively connecting the sub-circuit blocks **within each corresponding sub-circuit cell**" has been added to claims 1 and 9. This limitation finds support in paragraphs [0022]-[0024], and in Fig. 3 for instance, and no new matter is introduced. According to the method recited in claims 1 and 9 of the instant application, the connection layer is used to create a connection within each corresponding sub-circuit cell by selectively connecting the sub-circuit blocks **within each corresponding sub-circuit cell**. Therefore, Therefore, the connection selectively connects the sub-circuit blocks within each sub-circuit cell (the connection between the sub-circuit blocks is made with the same sub-circuit cell), so that the sub-circuit cells in different positions

implement different circuit functions.

Different from the method of claims 1 and 9, Schadt uses two types of connectivity structure in order to integrated SLBs (interpreted as the sub-circuit blocks of the present invention) with the rest of the chip (col. 4, lines 42-56, Fig. 9). Specifically, Schadt uses the connectivity structure to create a connection between the SLBs and other portion of the chip/PLD e.g. I/O buffers, programmable logic core or memory blocks, but he fails to teach use the connectivity structure to create a connection between the SLBs within the same sub-circuit cell. Therefore, Schadt's method is patentably distinct from that of the present application, and reconsideration of claims 1 and 9 is politely requested.

Claims 2-3, 5, 7, 8, 10, 12, 14, 15:

Claims 2-3, 5, 7, 8 are dependent on claim 1, and therefore should be allowed if claim 1 is found allowable. Reconsideration of claims 2-3, 5, 7, 8 is politely requested.

Claims 10, 12, 14, 15 are dependent on claim 9, and therefore should be allowed if claim 9 is found allowable. Reconsideration of claims 10, 12, 14, 15 is politely requested.

3. Rejection of claims 6 and 13 under 35 U.S.C. 103 (a) as being unpatentable over Schadt et al. (US 6,870,395) in view of Maeda (US 6,052,014):

Response:

Claim 6:

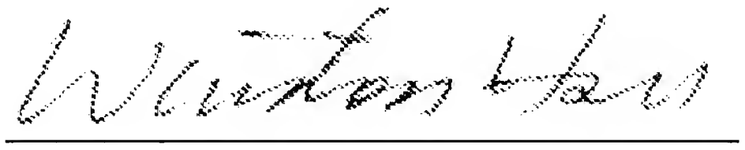
Claim 6 is dependent on claim 1, and therefore should be allowed if claim 1 is found allowable. Reconsideration of claim 6 is politely requested.

Claim 13:

Claim 13 is dependent on claim 9, and therefore should be allowed if claim 9 is found allowable. Reconsideration of claim 9 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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